APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,560	12/27/2001	Masayuki Takeshige	108075-00072	9892

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EXAMINER
BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/026,560	TAKESHIGE ET AL.
		Examiner	Art Unit
		Cynthia Britt	2133

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .
2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-18_ is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-18_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on _27 December 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☒ All   b)☐ Some * c)☐ None of:
       1.☒ Certified copies of the priority documents have been received.
       2.☐ Certified copies of the priority documents have been received in Application No. _____ .
       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
          application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)
1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____ .
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail. Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____ .

DETAILED ACTION

Claims 1-18 are presented for examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35

U.S.C. 119(a)-(d). The certified copy has been received.

Specification

The abstract of the disclosure is objected to because line 1 states "method and

system for shorten time ..." either 'for' should be 'to' or 'shorten' should be 'shortening'.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.

    4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sim et al. U.S. Patent No. 6,546,511 in view of Brauch et al. U.S. Patent No. 6,550,023.

As per claim 1, Sim et al. substantially teach the claimed method for testing memory circuits. In which functional blocks (including memory circuits) are tested in parallel and the results are compared to each other to determine if all results are the same. If the comparison indicates that all the outputs from the compare are the same, a single one of the outputs is sent to a failure discriminator, which compares the output with an expected output. (Figure 2, column 1 line 56 through column 2 line 24, claim 10) Not explicitly disclosed is that the comparison is made by comparing read data to write data.

However, in an analogous art, Brauch et al. teach that the general operation of each BIST memory test involves performing a series of writes via data input lines and

reads via data output lines to and from an addressed location. At various points in the test, the contents of the addressed location are read and compared to an expected value for the location at that point in the test. (Column 3 lines 23-39) Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of memory testing of Sim et al. with the comparison of Brauch et al. This would have been obvious because in order for a memory to function properly, it would be necessary for it to be able to read out the same data that written into it.

As per claim 2, Sim et al. teach that when the outputs of the memory (functional block) are the same, one of the outputs is sent to the failure discriminator (column 2 lines 5-6, column 3 line 36-41 and lines 50-55, column 4 lines 5-12).

As per claims 3-5, Brauch et al teaches that the compare results are stored and the read data is stored. A BIST functional block generates an address. The BIST functional block performs a series of operations at each address generated. The BIST functional block either generates or chooses input data, or generates or chooses expected data corresponding to the data previously written to the address generated. If the current operation is a write operation, the input data is written to memory on data input lines at the address generated. If the current operation is a read operation, the contents of memory at the address generated are read out on data output lines. A determination is made whether the current operation is a write or a read. If the current operation is a read, fault locator compares the output data read with the expected data. A determination is made as to whether the output data and expected data match. If a

mismatch occurs, the test is paused to allow the mismatch information to be retrieved.

After the mismatch is retrieved, either for example via external communication port or by

storing the mismatch information in another storage area on the chip, the memory test is

resumed. Upon resuming the test, or if it is determined that the output data matches the

expected data or if it is determined that the current operation is a write operation, a

determination is made as to whether more operations in the memory test exist. If more

operations exist, the next operation is obtained and some are repeated until no more

operations exist for the current address. (Figure 3 column 5 lines 17-60, claim 1)

Claims 6-8, 10, and 14-15 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Sim et al. U.S. Patent No. 6,546,511 in view of Usui U.S. Patent

No. 5,793,774.

As per claims 6 and 14, Sim et al. substantially teach the claimed system and

device for testing memory circuits. In which functional blocks (including memory circuits)

are tested in parallel and the results are compared to each other to determine if all

results are the same. If the comparison indicates that all the outputs from the compare

are the same, a single one of the outputs is sent to a failure discriminator, which

compares the output with an expected output. (Figure 2, column 1 line 56 through

column 2 line 24, claim 10) Not explicitly disclosed is the use of address decoders,

multiplexers, and that the comparison is made by comparing read data to write data.

However, in an analogous art, Usui teaches that typically used as the control

means is a microprocessor (CPU) such as one-chip microprocessor which incorporates

a RAM, a ROM, a timer, an I/O controller and the like. Alternatively, the control means

may be any bus master. The memory controlling means employs logic devices in

combination and is adapted to control the operations of the first memory and storage

means to output a chip select signal. The chip select signal permits or inhibits the

access to the first memory for the read-out or write-in operation. The command

sequence detecting means detects address decoding, address detection, data detection

and the start and end of a command sequence. The command sequence detecting

means typically employs logic devices in combination. The selecting means includes a

multiplexer (MUX) as a main component and several logic devices employed in

combination to realize a selective connection of the two paths (column 4 line 66 through

column 5 line 4, column 5 lines 31-42, and column 6 lines 26-39). Therefore it would

have been obvious to a person having ordinary skill in the art at the time this invention

was made to have used the testing method of Sim with the data accessing method of

Usui. This would have been obvious as suggested by Usui since these are 'typical'

methods used for accessing the data.

As per claims 7, 8 and 15, Usui teaches the memory control circuit decodes an

address sent from the CPU onto the address bus a to access the flash memory, the

memory control circuit asserts the select signals, and memory read signal or memory

write signal to access the flash memory and SRAM. (Column 11 lines 20-25)

As per claim 10, Sim et al teach that the transmitter transmits one of the output signals

when the comparator determines the output signal levels to be the same and transmits

a defect signal when the comparator determines the output signal levels to be different.

The first checking portion (causing interrupt) does not output any of the least significant

bits (LSB) if the logic levels of the received bits are different. As in the first failure

discriminator, the second failure discriminator determines that the single chip is

defective if each of the checking portions does not output any LSB, or if the level of

each of the LSBs output from the checking portions are not equal to a predetermined

target level. In the structures and operations of each checking portion, each

checking portion comprises AND gates and an OR gate and a transmission gate 4.

(Figures 3 and 4 column 2 lines 10-15 and column 4 line 20 through column 5 line 18)

Claims 9, 11-13, and 16-18 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Sim et al. U.S. Patent No. 6,546,511 in view of Usui U.S. Patent

No. 5,793,774 as applied to claims 6 and 14 above, and further in view of Tomari

U.S. Patent No. 6,480,979.

As per claims 9,11-13,and 16-18 Sim et al. and Usui as combined above,

substantially teach the claimed system and device for testing memory circuits. In which

functional blocks (including memory circuits) are tested in parallel and the results are

compared to each other to determine if all results are the same. If the comparison

indicates that all the outputs from the compare are the same, a single one of the outputs

is sent to a failure discriminator, which compares the output with an expected output.

(Sim et al. Figure 2, column 1 line 56 through column 2 line 24, claim 10) And that

typically used as the control means is a microprocessor (CPU) such as one-chip

microprocessor which incorporates a RAM, a ROM, a timer, an I/O controller and the

like. Alternatively, the control means may be any bus master. The memory controlling

means employs logic devices in combination and is adapted to control the operations of

the first memory and storage means to output a chip select signal. The chip select

signal permits or inhibits the access to the first memory for the read-out or write-in

operation. The command sequence detecting means detects address decoding,

address detection, data detection and the start and end of a command sequence. The

command sequence detecting means typically employs logic devices in combination.

The selecting means includes a multiplexer (MUX) as a main component and several

logic devices employed in combination to realize a selective connection of the two paths

(Usui, column 4 line 66 through column 5 line 4, column 5 lines 31-42, and column 6

lines 26-39). Not explicitly disclosed is that the compare circuitry contains a memory for

holding the results of the comparison.

However, in analogous art, Tomari teaches that a semiconductor integrated-

circuit device includes both conventional internal circuitry, and a selection circuit that

provides external output of signals from the internal circuitry under control of a selection

signal. Each device has an internal test circuit that carries out tests in response to test

control codes received from a tester, evaluates the response signals from the internal

circuitry, makes a pass/fail decision, and provides the tester with the pass/fail result.

The semiconductor device comprises internal circuitry implementing the functions that

the semiconductor device provides when used as a product, and an internal test circuit

that tests the internal circuitry. The internal test-circuit includes a test result retention

circuit. (Abstract, column 11 lines 44-54, and Figure 10) Therefore it would have been

obvious to a person having ordinary skill in the art at the time this invention was made to have used the result retention circuit of Tomari with the testing circuitry of Sim et al. and Usui as combined above. This would have been obvious as all data read in or read out would necessarily be "temporarily stored" in the scan latches (memory/storage) on the way into the comparator or on the way out.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,539,699   Sato et al.

This patent teaches a flash memory-testing apparatus is capable of testing a flash memory while maintaining the conventional memory test functions. The flash memory testing apparatus obtains the number of programming pulses applied to each address of the flash memory. The flash memory testing apparatus executes the following steps: comparing a readout data of the flash memory under test under a writing or erasing test with an expected data output from a test pattern generator, outputting a failure signal to a failure analysis memory to store the failure data in a memory part in the failure memory in case where readout data does not coincide with an expected data, and outputting a pass signal when the readout data coincides with the expected data. The flash memory testing system has a counter for counting the number of programming pulses or erasing pulses and supplying the count data to the memory part of the failure analysis memory.

"Processor-Programmable Memory BIST for Bus-connected Embedded Memories" Tsai

et al. Design Automation Conference Proceedings,

Publication Date: 30 Jan.-2 Feb. 2001 pages: 325 - 330 Inspec Accession Number:

6924510

This paper presents a processor-programmable built-in self-test (BIST) scheme

suitable for embedded memory testing in the system-on-a-chip (SOC) environment. The

proposed BIST circuit can be programmed via an on chip microprocessor. Upon

receiving the commands from the microprocessor, the BIST circuit generates pre-

defined test patterns and compares the memory outputs with the expected outputs.

Most popular memory test algorithms can be realized by properly programming the

BIST circuit using the processor instructions. Compared with processor-based memory

BIST schemes that use an assembly-language program to generate test patterns and

compare the memory outputs, the test time of the proposed memory BIST scheme is

greatly reduced.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391.

The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

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